RESEARCH ARTICLE OPEN ACCESS

Pass transistor Based Negative Edge Trigged D Flip Flop (PTDFF)

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Abstract
In this paper a new technique is proposed based on the comparison between Conventional Transistorized Flip-flopand Data transition Look ahead D flip flop here we are checking the working of DLDFF and the conventional D Flip-flop after that we are analyzing the characteristic comparison using power & area constraints after that we are proposing a Negative Edge triggered flip-flop named as Passtransistor based negative edge trigged D Flip Flop(PTDFF) with reduced number of transistors which will reduce the overall power area as well as delay. The simulations are done using Microwind& DSCH analysis software tools and the result between all those types are listed below. Our proposed system simulations are done under 50nm technology and the results are tabulated below. In that our proposed system is showing better output than the other flip-flops compared here.

I. INTRODUCTION

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.

Flip-flops can be either simple (transparent or opaque) or clocked (synchronous or edge-triggered); the simple ones are commonly called latches.

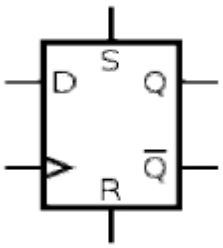

Fig 1: D flip-flop symbol

The D flip-flop is widely used. It is also known as a data or delay flip-flop.The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line.

Most D-type flip-flops in ICs have the capability to be forced to the set or reset state (which ignores the D and clock inputs), much like an SR flip-flop. Usually, the illegal S = R = 1 condition is resolved in D-type flip-flops. By setting S = R = 0, the flip-flop can be used as described above.

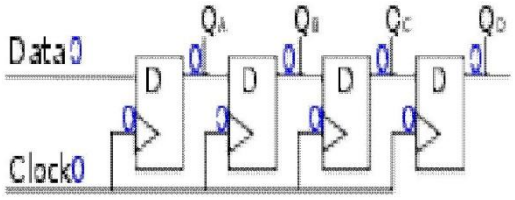

Fig2 :4-bit serial-in, parallel-out (SIPO) shift register

These flip-flops are very useful, as they form the basis for shift registers, which are an essential part of many electronic devices.

The advantage of the D flip-flop over the D-type "transparent latch" is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. An exception is

that some flip-flops have a "reset" signal input, which will reset Q (to zero), and may be either asynchronous or synchronous with the clock.

The above circuit shifts the contents of the register to the right, one bit position on each active transition of the clock. The input X is shifted into the leftmost bit position.

Types of D Flip-Flops

i) Classical Negative-edge-triggered D flip-flop
ii) Master–slave pulse-triggered D flip-flop
iii) Edge-triggered dynamic D storage element

II. CONVENTIONAL LOW POWER D FLIP-FLOP

Flip-Flops are the basic elements for storing information and they are the fundamental building blocks for all sequential circuits. Flip-flops, have their content change only either at the rising or falling edge of the enable signal. But, after the rising or falling edge of the enable signal, the flip-flop's content remains constant even if the input changes. In a conventional D Flip Flop shown in Fig 2, the clock signal always flows into the D flip-flop irrespective of whether the input changes or not. Part of the clock energy is consumed by the internal clock buffer to control the transmission gates unnecessarily. Hence, if the input of the flip-flop is identical to its output, the switching of the clock can be suppressed to conserve power.

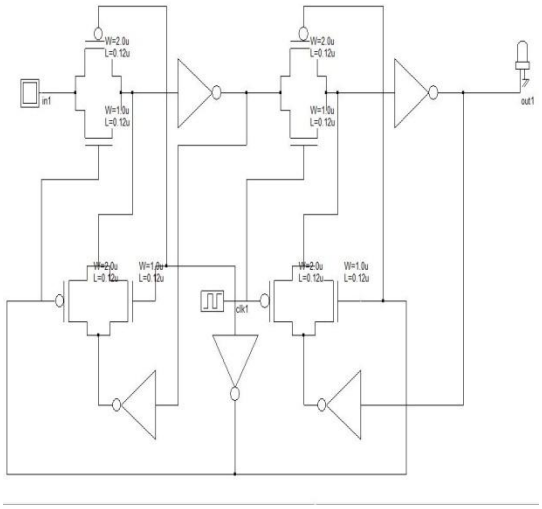

Fig3 : Conventional D Flip-flop Design

III. DLDFF

In a DLDFF shown in Fig 3, the gating function is derived within the flip flop without any external control signal. The external clock signal of the flip-flop still switches. But, the clock signal flowing into the flip flop is deactivated when there are no data transitions. Generally flip- flop finds its best application in the counters. Counters can be classified as synchronous and asynchronous counters based on the application of clock to the flip-flops. A synchronous counter is clocked by a single clock for all the stages and the output for each stage changes at the same time.

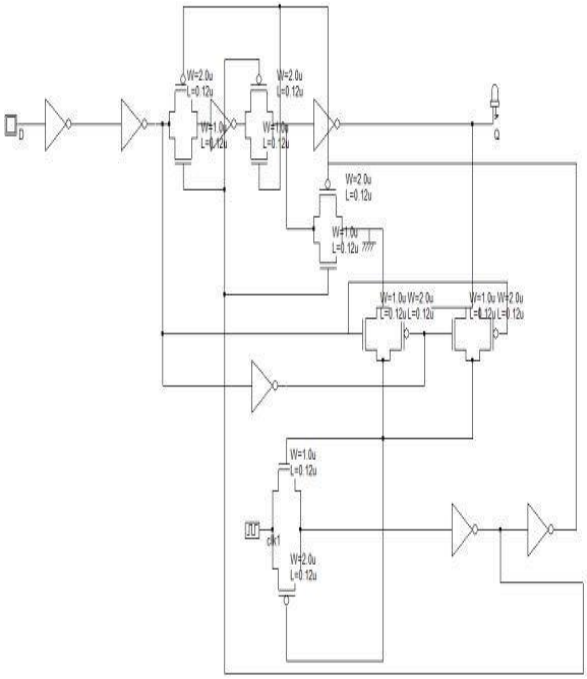

Fig 4: Data transition Look ahead D Flip-Flop

IV. OUR PROPOSED NEGATIVE EDGE TRIGGERED FLIP-FLOP DESIGN (STDFF)

Edge-triggered flip-flops are becoming a popular technique for low-power designs since they effectively enable a halving of the clock frequency. A dual pulse clock generator is needed to generate pulses at both rising and falling edges of a low-swing clock. This Particular clock pulse is used to switch the ground of the flip-flop circuit. This ground will be utilized by the NMOS and PMOS connected directly to the D input of the circuit. The Proposed system is shown in the Fig below.

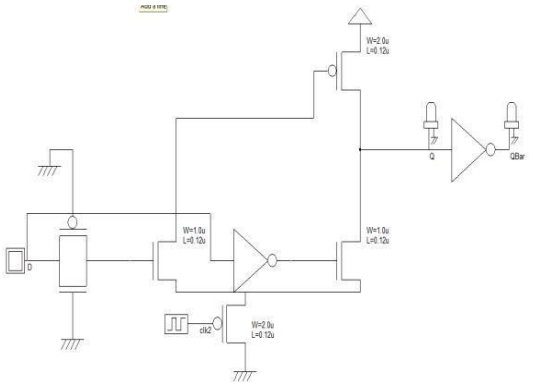

Fig 5: Our Proposed Negative Edge Triggered flip-flop

By using the Transistor switching logic only we are designing this circuit so it will be consuming only less power when compared to all other circuits. As well as we are having only 8 Transistors including the not gates also. So we will be having much reduced power and area when compared to the other two designs. At the same time due to the reduced no of transistor count we can reduce the delay oriented

V. IMPACT OF PTL ON AREA ,POWER AND DELAY:

Power reduction is a serious concern now days. As the MOS devices are wide spread, there is high need for circuits which consume less power, mainly for portable devices which run on batteries, like Laptops and hand-held computers. The Pass-Transistor Logic (PTL) is a better way to implement circuits designed for low power applicati

The power consumption in a circuit can be decreased by reducing:

- Switching activity in the circuit
- Switching capacitance of each node
- Supply voltage
- Short-Circuit Current

Let's look at a PTL design:

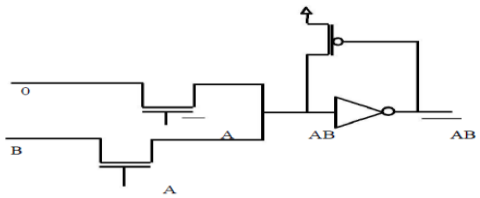

Fig 6: pass transistor logic gate

This kind of PTL design is called the Single-Rail Pass-Transistor Logic (also called LEAP). Here, a basic AND/NAND function is implemented. The PMOS transistor which is connected opposite to the output inverter is called a bleeder transistor, which is used to pull the weak '1' arriving at the input of the inverter.

Now, the advantage of PTL comes from the fact that it is best suitable to implement all the above power reduction techniques:

- Switching activity in the circuit can be reduced by eliminating the glitches. This can be done by controlling the delays of each pass transistor (controlling the widths and lengths).
- .Switching capacitance of a node in the PTL will be less when compared to a node in the CMOS design. Due to the smaller size of the transistors in PTL implementation.
- The lengths of the transistors should be as small as possible, because increased lengths result in more IR_{drop} across the transistor.
- The widths of transistors also should be small. It's because the improvement seen in the switching of that transistor will be subdued by the delay caused in the input, which is driving that wider gate. This phenomenon can be observed in the presentation slides.

Like the CMOS technologies, the supply voltage can be reduced at the cost of some increase in delay of the circuit.

There are fewer ground connections (only at the inverters) means fewer V_{DD} to GND connections during switching. So theoretically PTL implementation should draw least amount of short circuit power. Thus the Proposed Switching Transistor Based D Flip-flop design shows much less power & Area constraints than the Existing two Flip-Flop designs

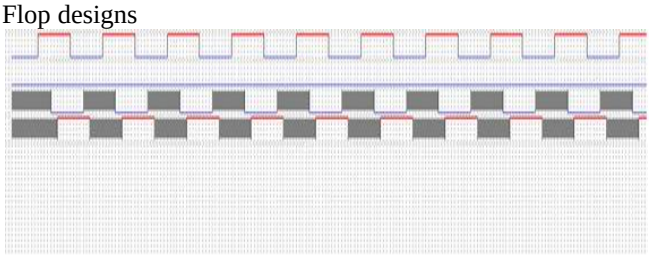

Fig7 : Waveform Output of the Proposed Negative Edge Triggered flip-flop

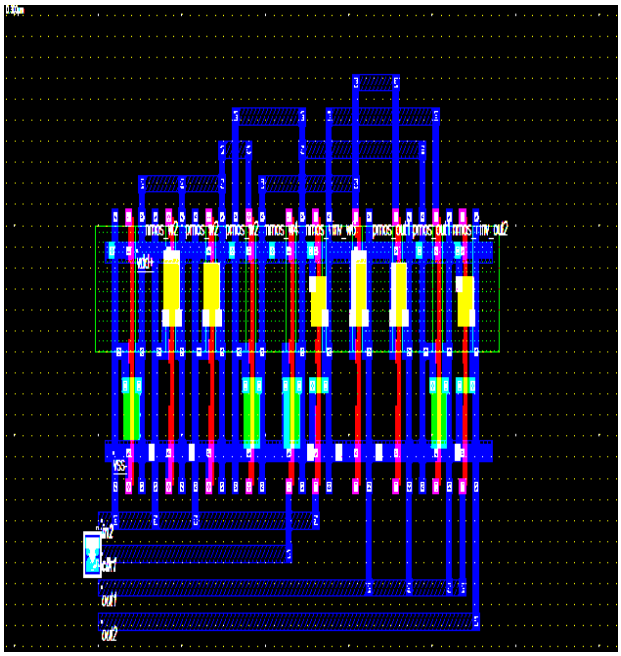

Fig8 :Layout of Proposed System

The graph represents the input & output characteristics of our proposed system from that we can clearly understand how it works as negative edge triggered flip-flop. There is some nano seconds delay is there even though it's a negligible amount only. Those delays can be further reduced by reducing the

sizes of the transistor we are using in this circuit. Or by reducing the nano meter technology also we can reduce the constraints. The Layout design of the proposed new flip-flop is shown in the Fig6 the area of that is mentioned at the downside of the layout. Power consumption characteristics is shown

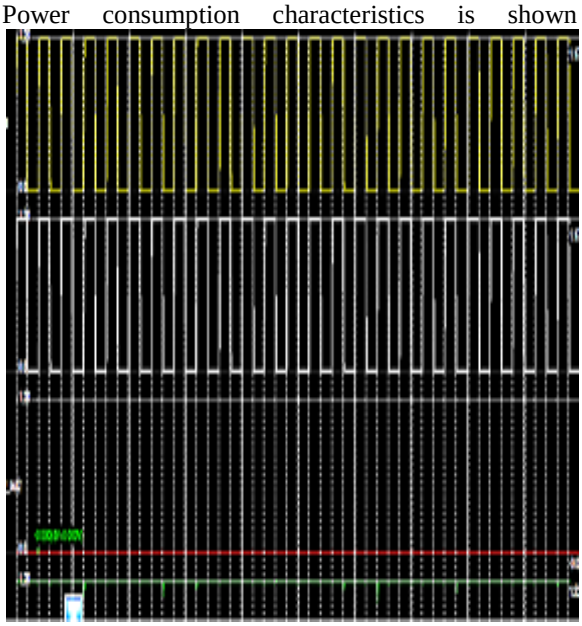

FIG 9: Power characteristics of proposed design

TABULATION

Area And Power Comparision Table:

Type	**Power Consumption**	**Area consumption**
DFF (90nm)	**0.898uw**	**15x12 um**
DFF(70nm)	**0.31uw**	**41x8um**
DFF (50 nm)	**0.768uw**	**55x8um**

Power & Area Comparison Table

Type	Power Consumption	Area Consumption
Conventional D Flip-Flop	90.07uW	25x14um^2
DLDFF	0.348mW	38x13um^2
Our Proposed Design(STDFF)	3.287uW	14x12um^2

VI. CONCLUSION

In this Paper we proposed a new D flip flop design which is named as Passtransistor based negative edge trigged D Flip Flop(PTDFF). The Proposed system shows 85% Power improvement than the Existing Data Transition look ahead D Flip-Flop and it shows an improvement of 40% in area constraints. Thus our proposed system is having very less power and area constraints which will lead to improvement in the case implementation in future mobile devices. This can be much suitable for application of battery oriented operation for less power and area. In future we can add some other leakage reduction techniques and the power can be further reduced.

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